Next Generation CMOS Active Pixel Sensors for satellite hybrid optical communications/imaging sensor systems

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ABSTRACT

Given the current choices of 1) an ever increasing population of large numbers of satellites in low-earth orbit (LEO) constellations for commercial and military global coverage systems, or 2) the alternative of smaller count geosynchronous satellite system constellations in high-earth (HEO), of higher cost and complexity, a number of commercial communications and military operations satellite systems designers are investigating the potential advantages and issues of operating in the mid-earth orbit altitudes (MEO) (between LEO and HEO). At these MEO altitudes both total dose and displacement damage can be traded against the system advantages of fewer satellites required. With growing demand for higher bandwidth communication for real-time earth observing satellite sensor systems, and NASA's interplanetary and deep space virtual unmanned exploration missions in stressing radiation environments, JPL is developing the next generation of smart sensors to address these new requirements of: low-cost, high bandwidth, miniaturization, ultra low-power and mission environment ruggedness. Radiation hardened/tolerant Active Pixel Sensor CMOS imagers that can be adaptively windowed with low power, on-chip control, timing, digital output and provide data-channel efficient on-chip compression, high bandwidth optical communications links are being designed and investigated to reduce size, weight and cost for common optics/hybrid architectures.

Keywords: APS, active pixel sensor, lasercom, hybrid-optical, MEO, radiation hardened/tolerant, optical communications

1. INTRODUCTION

Typically high bandwidth laser communication systems have separate focal planes for beacon acquisition, tracking and readout, due to changes in field-of-view (FOV) and the high bandwidth signal requirements of the readout detector. Figures 1a,b, & c show prototype designs leading to a combined arrangement for an optical communication/imaging system as well as imaging spectrometer [Ref. 1]. In an effort to develop lighter weight, lower power systems for more cost/weight/volume efficient satellites and spacecraft, JPL is developing technologies that will allow the same focal plane systems to operate both as a beacon tracker, as well as the high bandwidth signal readout. With the attendant reduction of weight, allowances for increased shielding may permit more radiation tolerant focal planes to be implemented. In the beacon acquisition/tracking mode, a star tracker reference unit (SRU) or other inertial monitoring unit (IMU) is used to point the axis of the optical system at the expected position of the planet and/or spacecraft/satellite transceiver. Though not in the scope of this paper, JPL is investigating the active pixel sensor discussed here to both provide a radiation insensitive SRU [Ref. 2], in addition to optical beacon tracking and readout on the same focal plane using multiple windowed operations. Here the advantage of varying the integration time for dim versus bright objects imaged onto the same focal plane will allow a high level of integration and functionality to be achieved. JPL is also actively involved with the next level of integration where an adjacent or monolithic processor chip would actually perform the calculations for the attitude quaterion with respect to the celestial sphere. Typical CCD imagers for optical laser communication and star tracking generally have masses of one to seven kg and consume three to ten watts of power. The motivation for the replacement of a mature CCD system includes:

Simplification of Hardware:

CCD chips require various clocking voltages (i.e., six or more different voltage levels) in order to support the use of repeated lateral transfer of charge in an MOS electrode based analog shift register to enable readout of photo generated signal electrons (with attendant inefficiencies in conversion). Off-chip signal chain electronics that provide correlated double sampling (CDS) for noise reduction and amplification and/or analog-to-digital conversion also dissipate significant power. High charge transfer efficiency (CTE) in CCDs is achieved using a highly specialized fabrication process that is not generally CMOS compatible. Because of the separate electronics needed to provide timing, clocking and signal chain functions, CCDs typically dissipate approximately 80 percent of the system power to drive high capacitance voltage swings from and to off-chip electronics. The active pixel sensor, on the other hand, consumes 10sX to 100sX less power than CCDs and require no special supporting chip electronics. Due to the inclusion of an on-chip to analog to digital converters, direct communication with an onboard computer as well as the possible inclusion of on-chip centroiding algorithms significantly decreases power consumption.

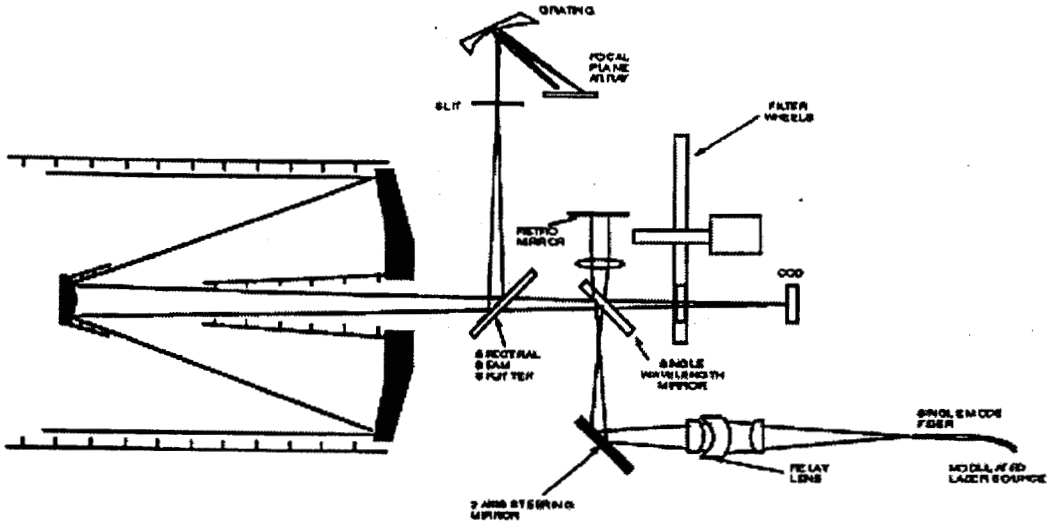


Figure 1a. Layout of combined optical communications terminal, imaging camera, & imaging spectrometer (Ref 1)

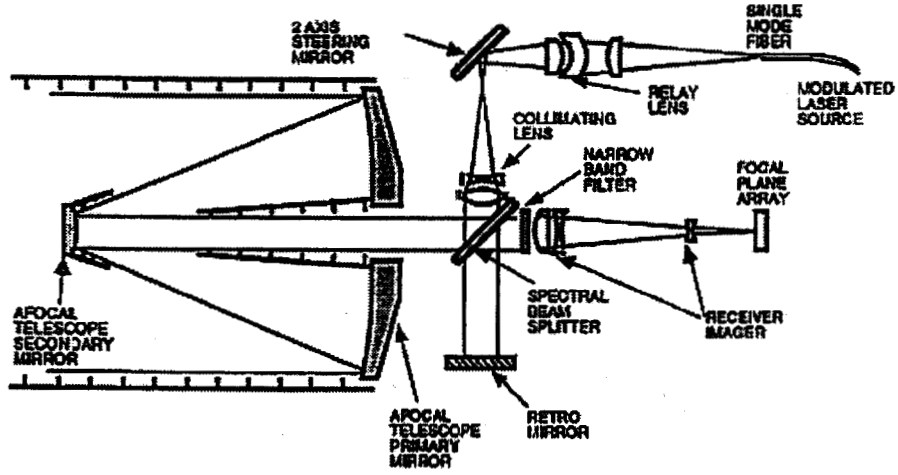


Figure 1b. Layout of the JPL Optical Communications Demonstrator (Ref 1)

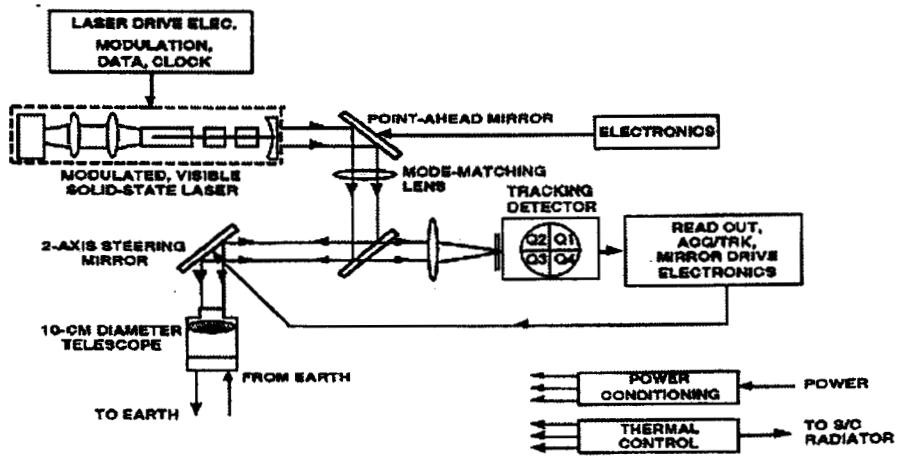


Figure 1c. Layout of the JPL Pluto Flyby Design (Ref 1)

No Image Blooming:

Due to the independent nature of the APS readout, image blooming generally present in CCDs when bright objects are present in the field of view is negligible with active pixel sensors. This is important for optical communications when orbiting spacecraft lie close to bright celestial bodies in the field of view of the sensor. This optical blooming problem is eliminated with the use of APS based laser communication focal planes. We have demonstrated at JPL collateral imaging of the -3 magnitude disk of Mars in the same field of view lying close to a 6 magnitude star, and no blooming occurred. This represents a dynamic range of 9 magnitudes which will be important for receiving distant beacons in the presence of bright celestial objects.

More Radiation Resistant:

Active pixel sensor technology that does not require hundreds to thousands of lateral transfers as with CCD technology reduces the centroid error noise due to proton induced displacement damage and charge trapping as can be seen in Figure 2. This is a problem in CCDs due to the statistical nature of this displacement damage mechanism so that a global correction that impacts the beacon centroid accuracy for optical communications occurs differently over separated areas of the CCD, and its correction is difficult, or intractable. Because of the direct addressing of each pixel in the APS sensor, this source of noise is all but eliminated. Although APS imagers generate dark current proportional to the total ionizing dose (consistent with most conventional CCDs), JPL is investigating the use of radiation hardened fabrication processes as well as careful pixel design, to avoid charge leakage due to "birdsbeak" effects, and various pixel photodiode and photogate architectures to investigate perimeter versus area parameters for pixel design and their effects on radiation sensitivity. In addition to pixel design, redundant and circuit threshold voltage compensation for digital timing control and analog operations is being investigated.

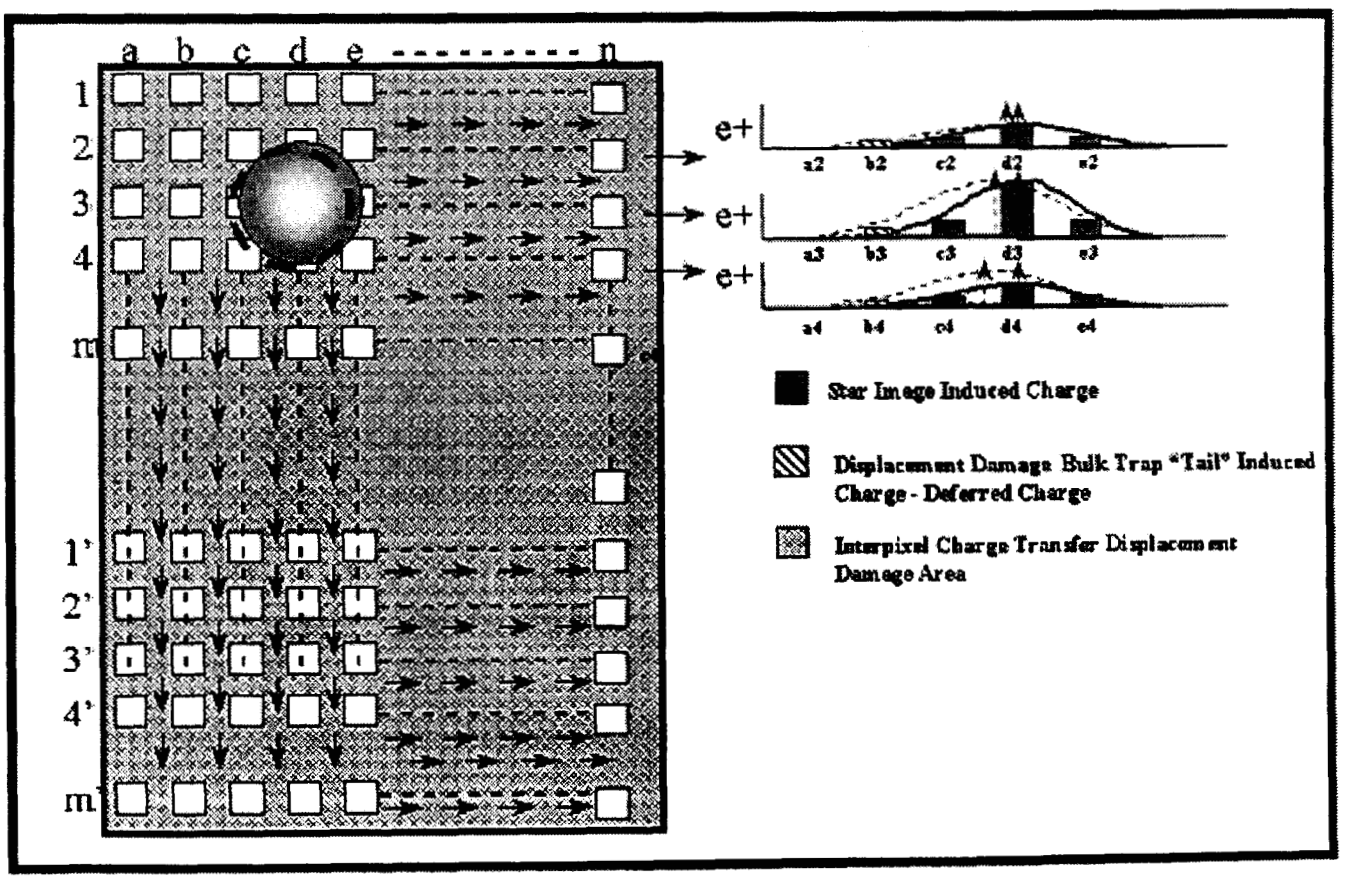


Figure 2. Laser communications CTE beacon boresight centroid error issues with CCD proton displacement damage.

2. APS TECHNOLOGY

An active pixel sensor is an imaging array with active transistors located with each pixel. Two types of APSs exist: photodiode pixel and photogate pixel. The 256x256 APS imager that was radiation tested is a 20.4 μm photodiode pixel with 3 transistors per pixel (shown in Figure 3a, as well as the on-chip output and selection electronics shown in 3b & 3c). Typical pixel pitch is ~15-17x the minimum feature size [3]-[9]. The sensors are fabricated in a standard CMOS process. The Hewlett-Packard 1.2 μm N-well CMOS process was provided through the MOSIS[1] service. The specific chip had a geometric fill factor of 20.8%. The conversion factor is approximately 3 μV/electron.

The power consumption of Very Large Scale Integration (VLSI) CMOS is intrinsically low, and locating the CMOS circuits for timing and control on chip eliminates high power chip to chip communication. The power consumption of our newest 512x512 digital camera is typically in the 13 mW range. Also, the CMOS will operate on a single 5 or 3.3 Volt supply.

Advancements in VLSI technology are easily incorporated onto a new APS. This includes the ability to provide additional functionality on a single chip (e.g., A/D conversion or potentially star centroid calculation). An example of state-of-the-art APS digital miniature cameras are depicted in Figures 4 & 5.

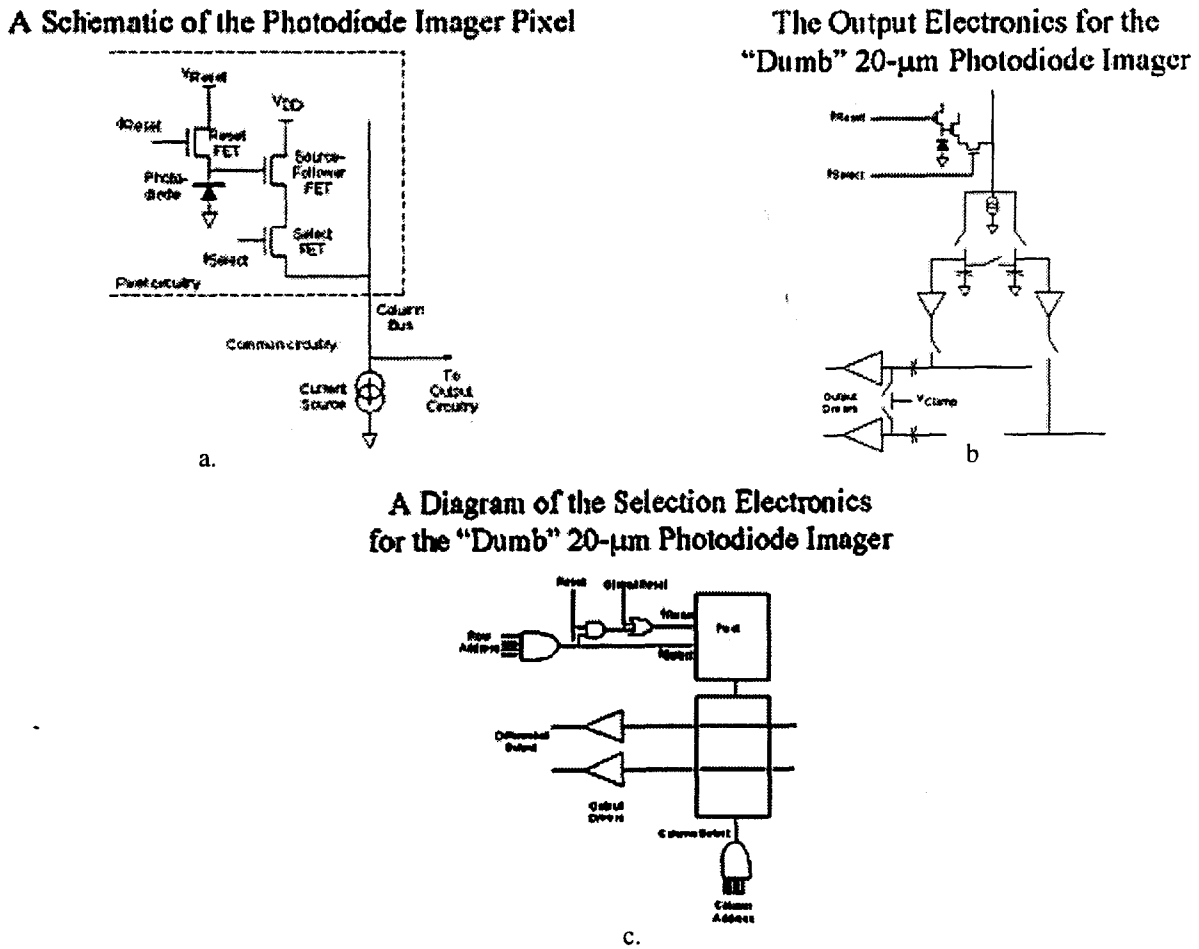


Figure 3. APS photodiode schematic, output and selection electronics for LM RHCMOS 5M process submission

[1] MOSIS aggregates designs from different sources onto one mask set, allowing designers to obtain small quantities and to share the cost of fabrication among a number of users.

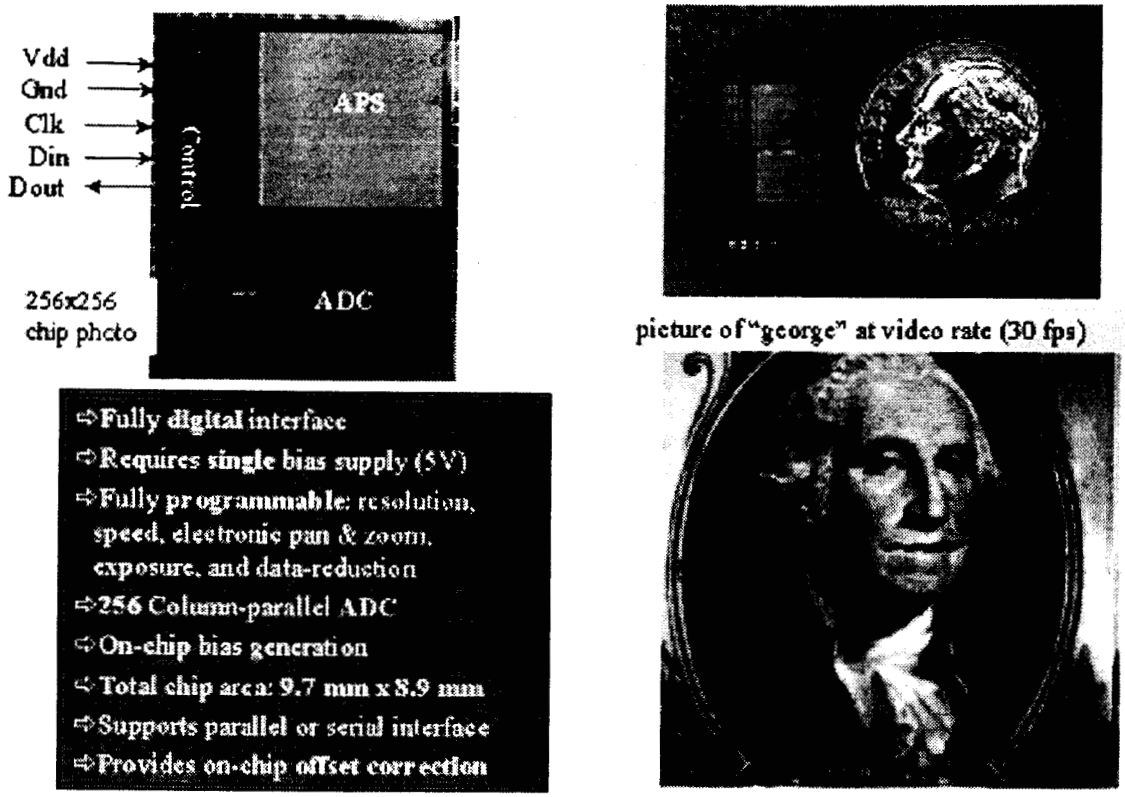


Figure 4. First fully digital camera on a chip: needs only FIVE wires for operation

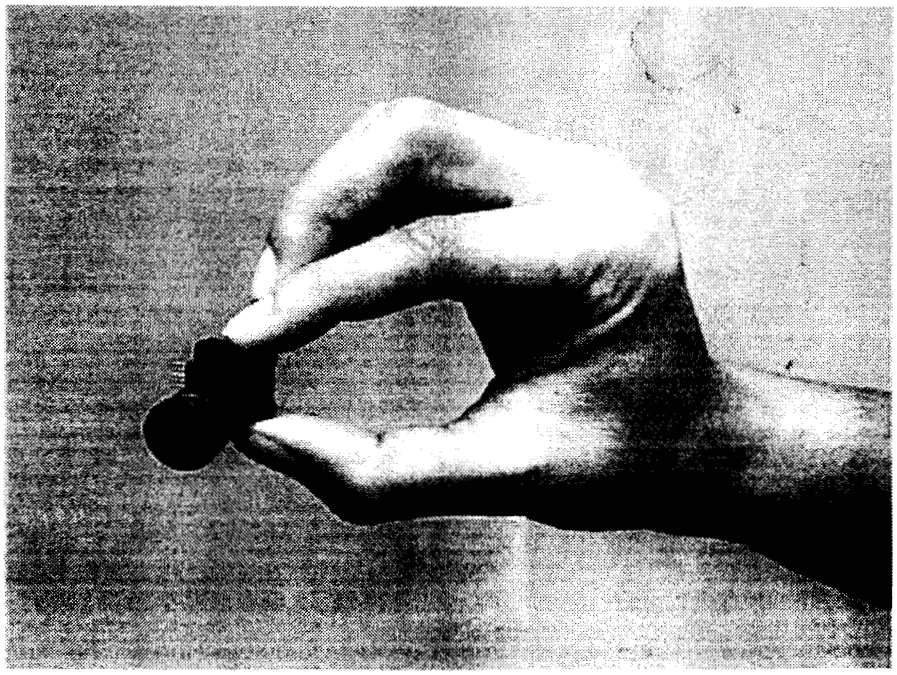


Figure 5. State-of-the-art 256x256 APS miniature digital camera (via 4 wires & ground)

3. NEXT GENERATION APS HYBRID OPTICAL COM/IMAGING SYSTEMS

Based on the current requirements for MEO altitude optical communications satellites, as well as solar explorations and missions to the outer planetary bodies (including Jupiter, its moons, i.e., Io and Europa, etc.), that require sustained exposure to radiation, JPL has been following an approach of a series of APS design, fabrication, test and evaluation efforts.

Potential advantages over CCD systems include:

- elimination of repetitive charge transfers which provides immunity to CTE degradation under radiation,
- device low current utilization that allows circumvention of latch up and single event upsets,
- on-chip signal processing that can be used to provide self-adjustments for centroiding, analog-to-digital conversion, and adjustment for radiation induced voltage level shifts.

Issues and problems to be addressed with silicon detectors include:

- Increased dark current generation due to radiation damage at the interfaces with the bulk,
- threshold shifts that induce loss of dynamic range,
- latch-up and single event upsets in timing/control in ADC circuits.

APS design approaches include:

- the development of innovative pixels for low dark current,
- the use of radiation-hardened foundry to develop a medium format "dumb" imager to iteratively develop optimal pixel structure,
- develop on-chip signal processing to self-adjust V_t shifts and dynamic range loss,
- develop radiation-hardened (SEU-circumventing) timing and control,
- develop radiation-hardened analog-to-digital converter (ADC),
- explore low temperature operation to identify optimal operating temperature for maximum radiation tolerance,
- develop large format, fully digital radiation-hardened APS at industrial foundries,
- test, evaluate and characterize performance,
- inject into state-of-the-art combined optical com/imaging system development test beds.

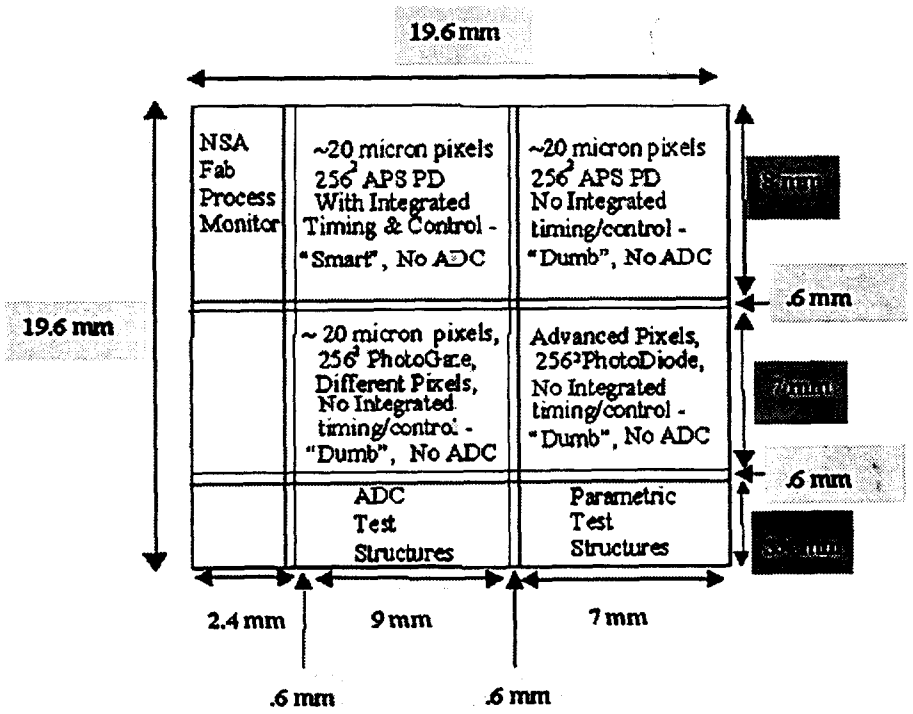


Figure 6. APS test device layout design for the Lockheed-Martin RHCMOS 5M Process

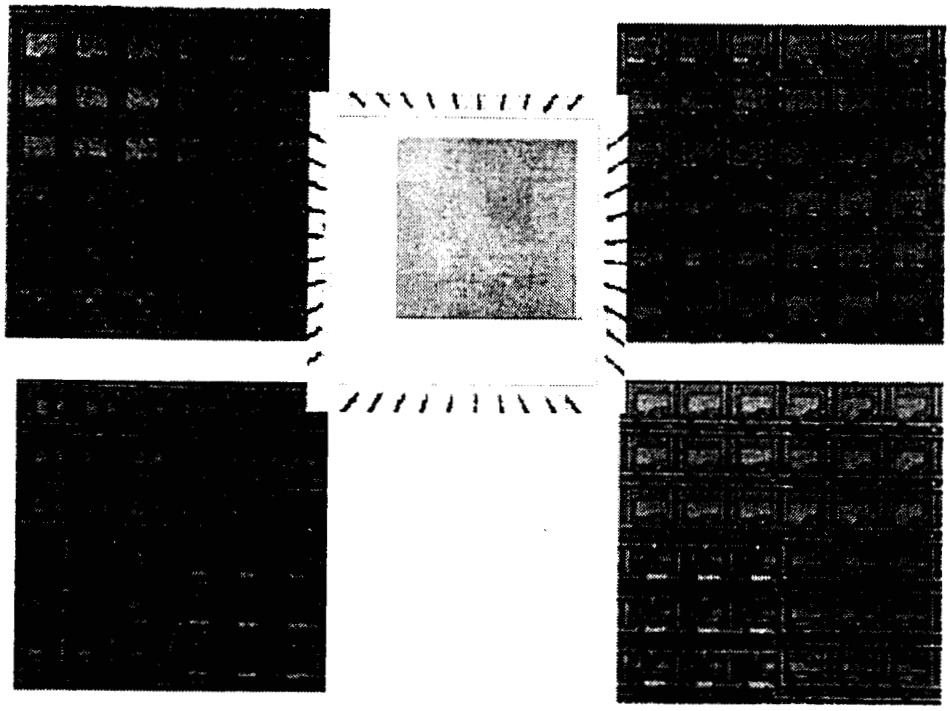


Figure 7. Chip Photograph & Micrographs of 16 Different Pixel Cell Test Designs

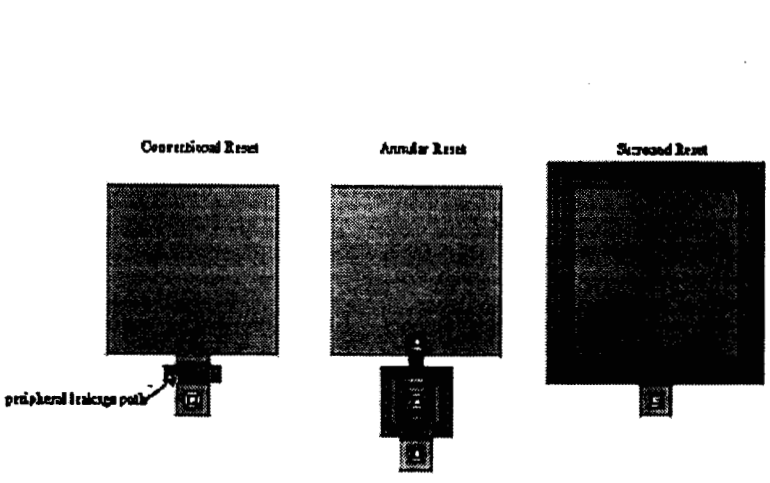


Figure 8a. Reset transistor layout options and

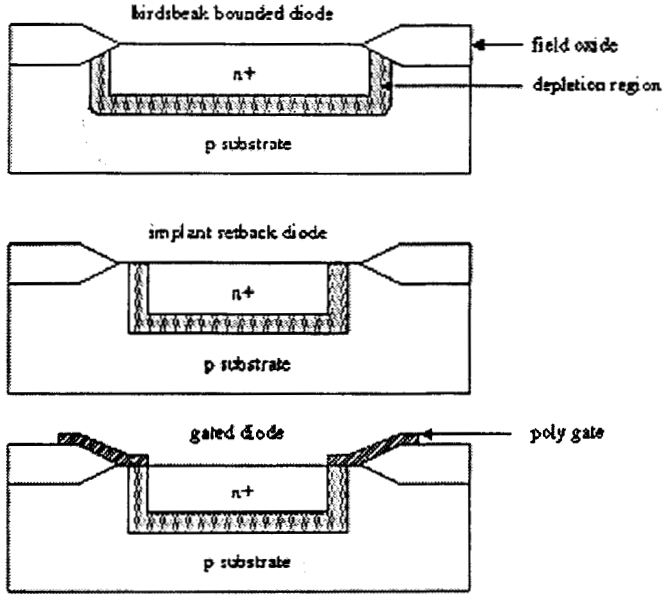


Figure 8b. Birdsbeak avoidance layout options

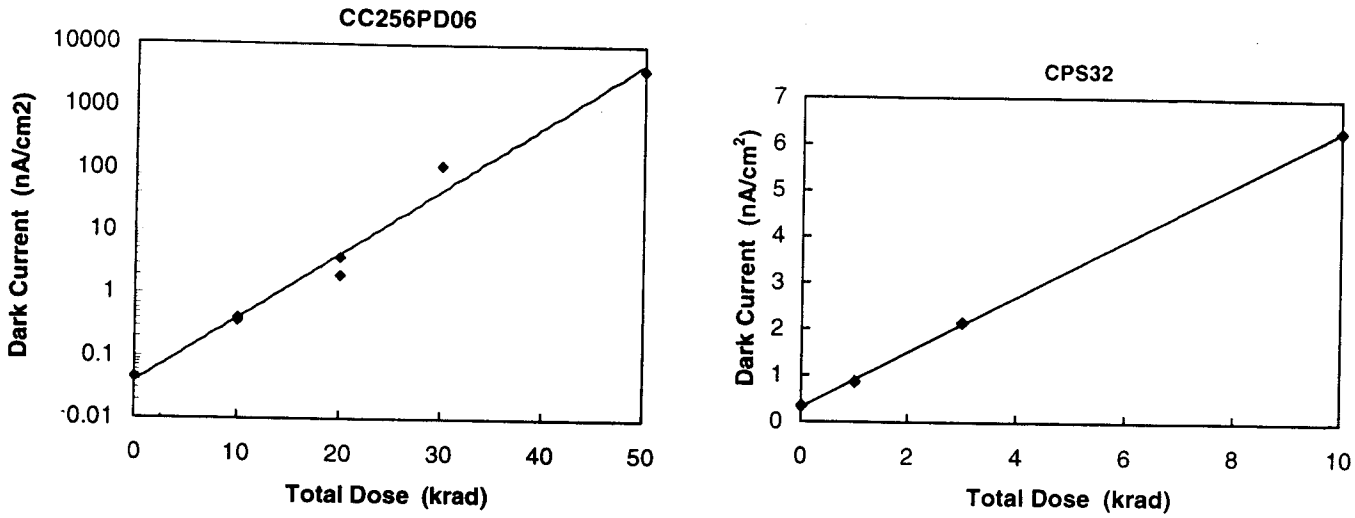
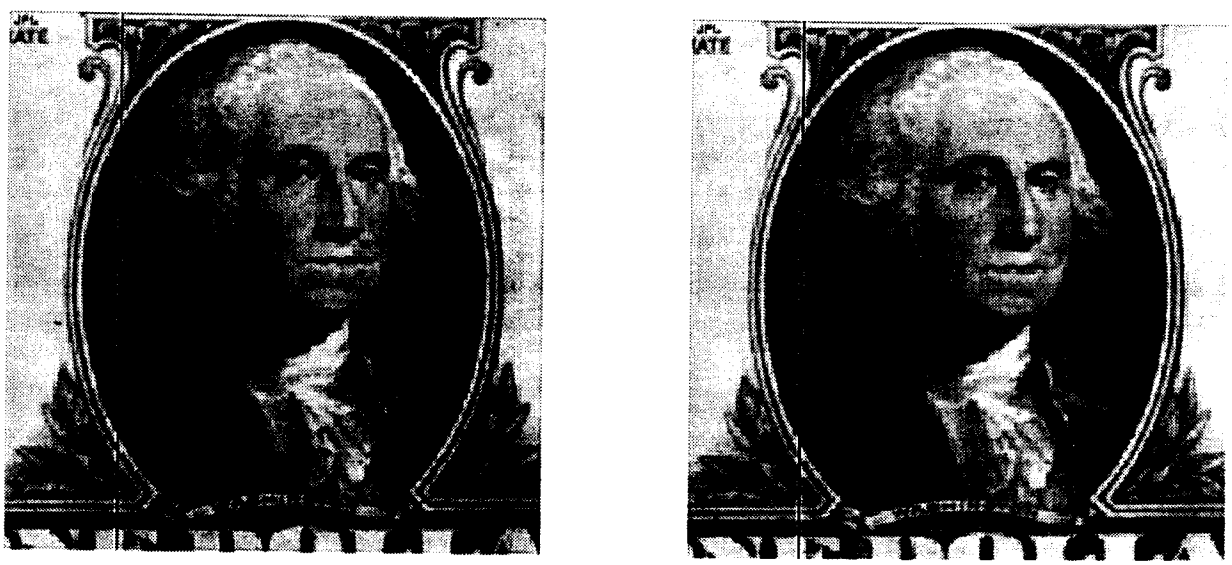


Figure 9. a. CC256 Imager APS, new results, 0.6μ MOSIS/HP, n+/p photodiode, birdsbeak bounded, Idark rises exponentially
b. CPS32 Charged Particle Sensor results reported at NSREC97, 1.2μ MOSIS/HP process, p+/n photodiode, gate bounded diode, Idark rises linearly with dose.



Pre-irradiation **Post-irradiation**

Figure 10. Tested at JPL Co60 facility: 10 krad total dose, Fully clocked, Room temperature exposure Results:Dark current increased 8x from 0.4 to 3.2 nA/cm^2· FPN increased to 6 mV RMS (due to dark current), Read Noise is unchanged (40e$^-$), small QE change in blue (10% reduction only).

4. RADIATION-HARDENED TEST METHODOLOGY.

The project involves the fabrication of what we have called several dumb APS imagers in the same reticule as smart imagers (those that have the on-chip timing and control). Figure 6 shows the APS device floor plan "layout" for the Lockheed Martin RHCMOS 5M process. By segmenting or progressively testing increasingly complex levels of integration, we will be able to understand the effects of different parameters on individual analog, digital, and parametric test structures that are the sub-units of the integrated imager in order to optimize both performance and decreased radiation sensitivity. This approach that is analogous to validating empirically derived pixel design has been successful in allowing low-cost, single run multiple design assessment studies that have allowed active pixel sensors to achieve nearly equivalent performance to commercial CCDs within only three years, as opposed to twenty years for CCDs to achieve the same level of imaging performance. Figure 7 shows microphotographs of a chip that was submitted to test 16 different pixel designs simultaneously. We have performed a number of radiation ground tests on standard HP fabricated active pixel sensors with results given in Figures 9a and 9b as well as Figure 10. We have also tested the single event upset (SEU) and latch up experienced by this HP processed chip at Brookhaven National Laboratories. The results of these tests indicate that in interstellar space these on-chip APS control electronics and registers would have an LET that infers they have an upset rate of once every thousand years. The pixel test structures that will be characterized will determine the radiation effects due to:

- perimeter effects
- area effects
- corner effects
- silicide effects
- epitaxial thickness effects

In order to optimize the design, we will vary:

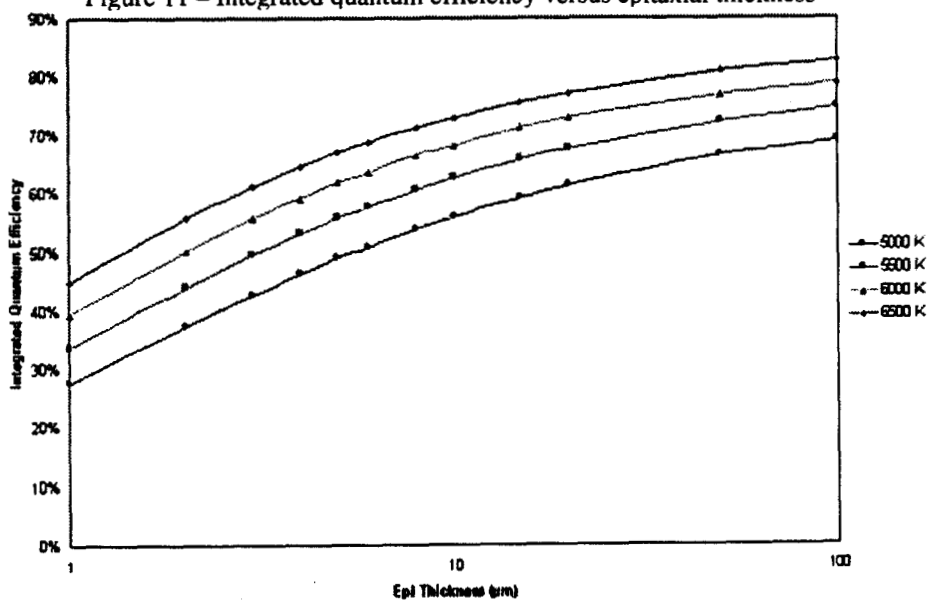
- the gate overlap region,
- implant setback,
- birdsbeak bounding

The thin oxide interface state dark current is controlled by Shockley-Hall-Read noise through the mid-gap states where the depletion region intercepts the silicon/silicon-interface as defined by

$$J = \pi kTqn_i\sigma n_{th}D_{it}$$

where D_{it} is the density of states at mid-gap. This differs from n_{it}, the parameter usually reported which is the total number of interface states. Figures 8a and 8b show various transistor layout options and a crossection of how implant setback and the poly gate may be employed to avoid a birdsbeak bounded diode. Varyingthe epi thickness of several of the wafers in the fab lot, as shown as shown in Figure 11, will allow a parametric study of the optimum epitaxial thickness (for increased responsivity) versus radiation sensitivity and noise to be assessed for various levels of radiation exposure in order to determine the best tradeoff in pixel designs and epitaxial thicknesses.

Figure 11 – Integrated quantum efficiency versus epitaxial thickness



5. SUMMARY AND CONCLUSION

JPL's current APS work that has demonstrated on-chip timing, control, analog-to-digital conversion, snap-shot mode with variable windowing, and large active pixel sensor arrays have just this year been integrated into a true camera-on-a-chip, with the development the digital integrated camera experiment (DICE) efforts for both 512x512 and 256x256 imagers. It is anticipated that a number of on-chip operations for laser communications, to reduce the off-chip processing will be demonstrated for beacon centroiding for miniaturized hybrid optical space satellite systems. The importance of these sensors that are expected to provide total dose and displacement damage hardness is key for the wide use for both cost-effective, commercial global coverage MEO satellite systems, as well as for weight and power efficient radiation-hardened imagers, high bandwidth laser communication systems, imaging spectrometers, and star tracker/imagers of the future.

6. ACKNOWLEDGEMENTS

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